

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	APU DDRIII MEMORY
05	APU CONTROL
06	APU GFX, GPP, UMI I/F
07	APU POWER & GND
08	DDRIII CHANNEL A
09	DDRIII CHANNEL B
10	HUDSON D4 UMI/PCIE/PCI/LPC/CPU
11	HUDSON D4 ACPI/USB/GPIO/AUDIO
12	HUDSON D4 SATA/SPI/RGB
13	HUDSON D4 POWER & GND
14	PCI EXPRESS x16 ,x1
15	PCI EXPRESS x4, VGA CONNECTOR
16	PCI SLOT
17	ITE 8620 , KB/MS. HWMO,TPM
18	F_USB, F_USB30 ,R_USB30
19	FAN/COM/LPT/MOSFET HOT
20	ALC887-VD2 CODEC
21	AUDIO JACK
22	ATX, FRONT PANEL
23	POWER SEQUENCE
24	VCORE (PWM ISL6377)
25	VCORE MOS

[illegible]

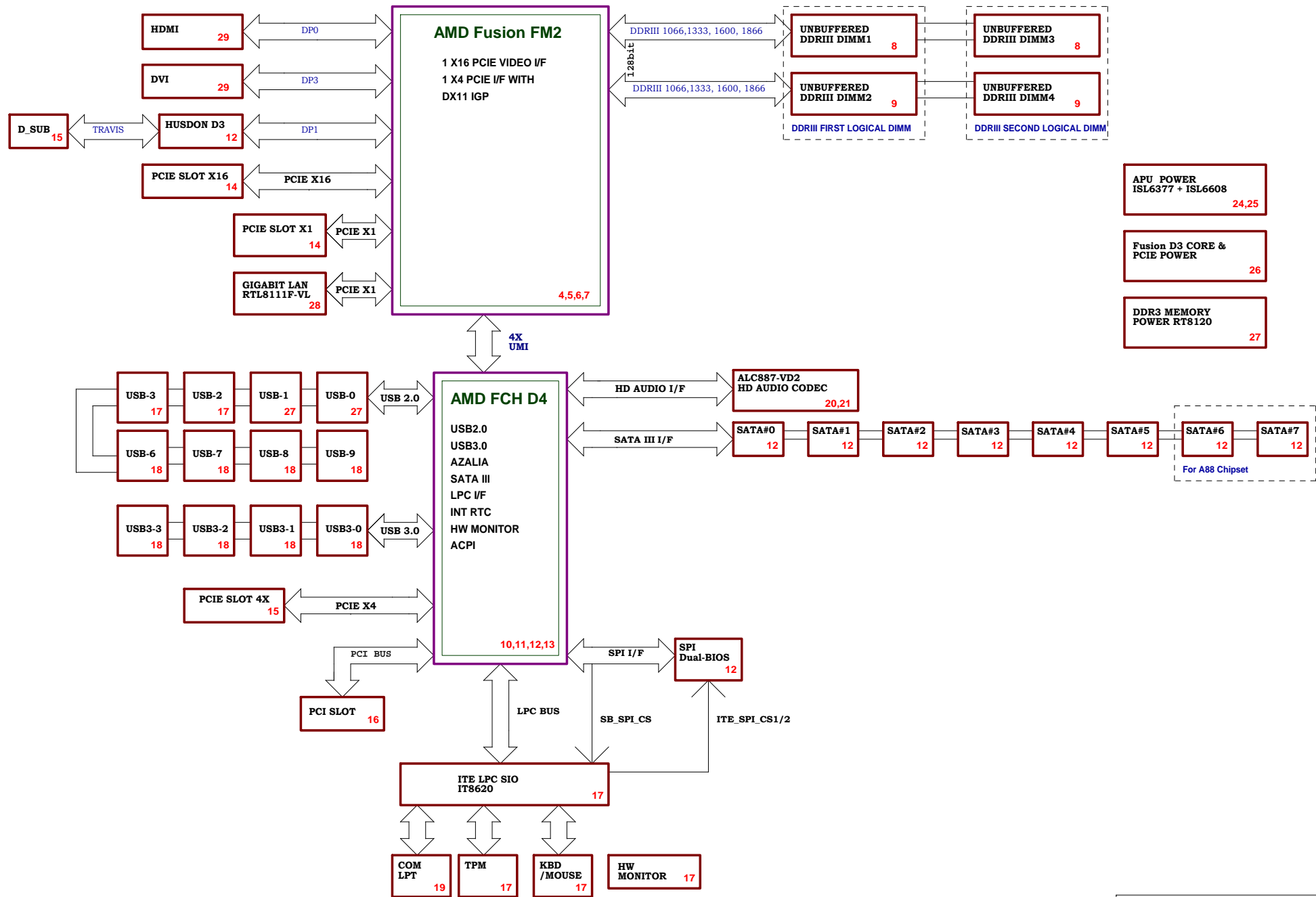
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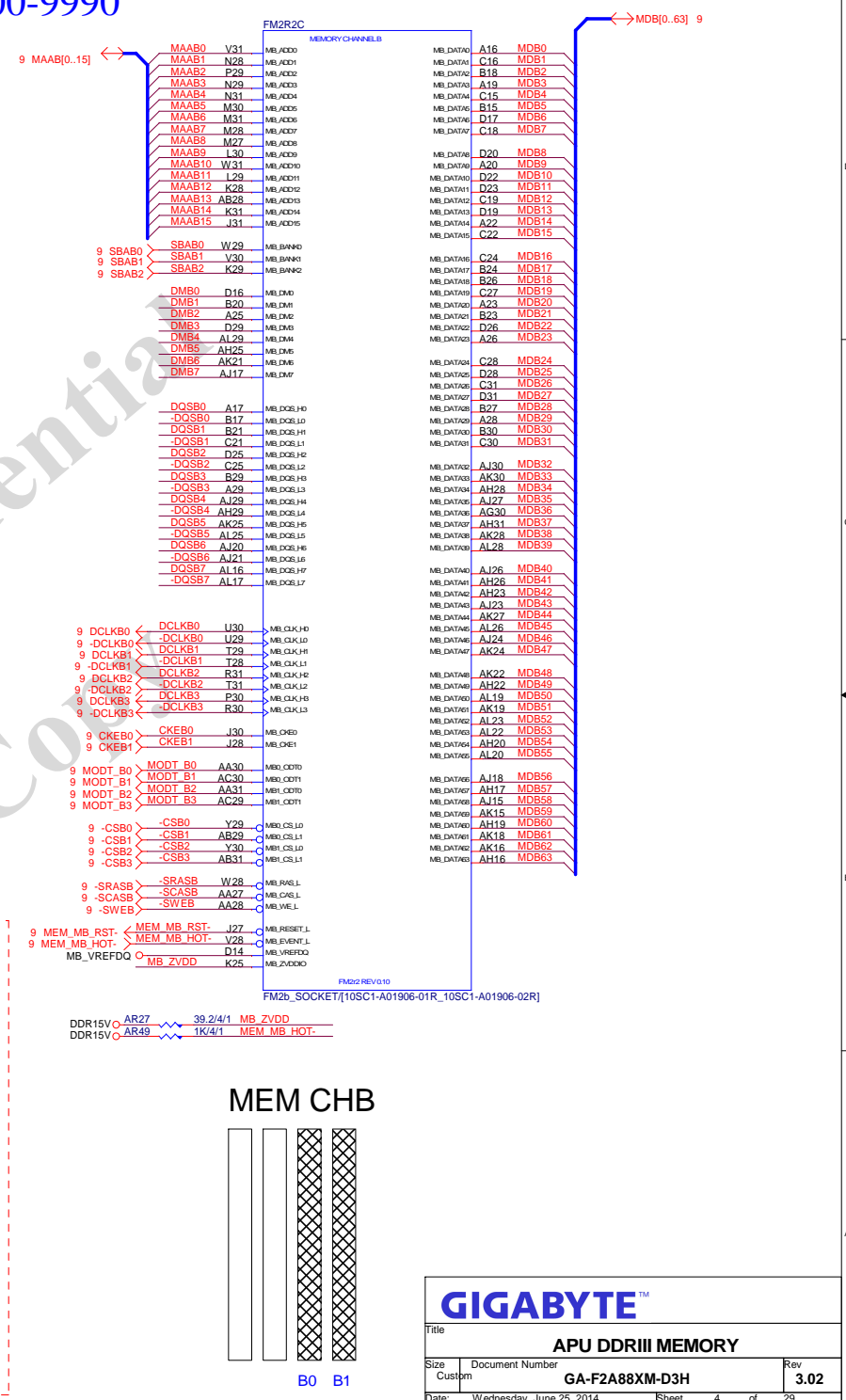
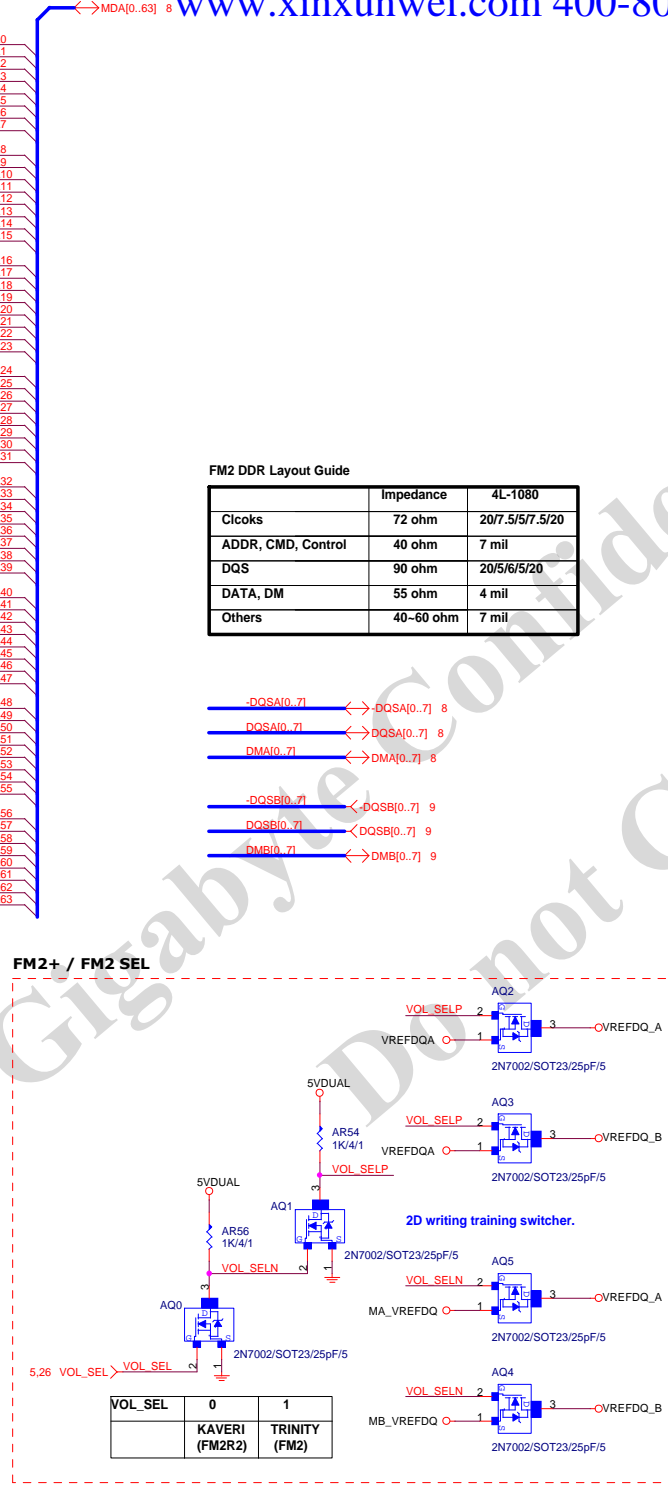
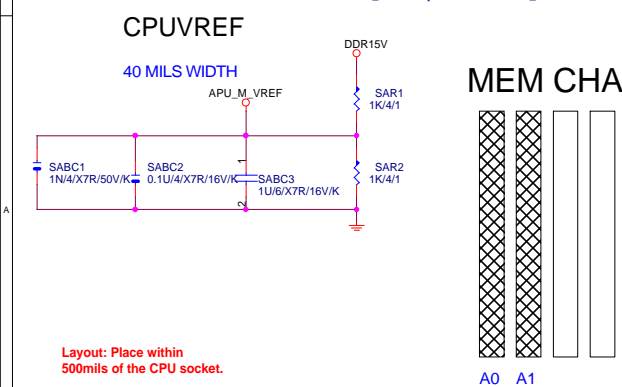
APU_VDDIO_SUS=DDR15V
APU_VTT_SUS=DDRVTT
APU_VDDP_RUN=APU_VDDR_RUN=APU_VDDP

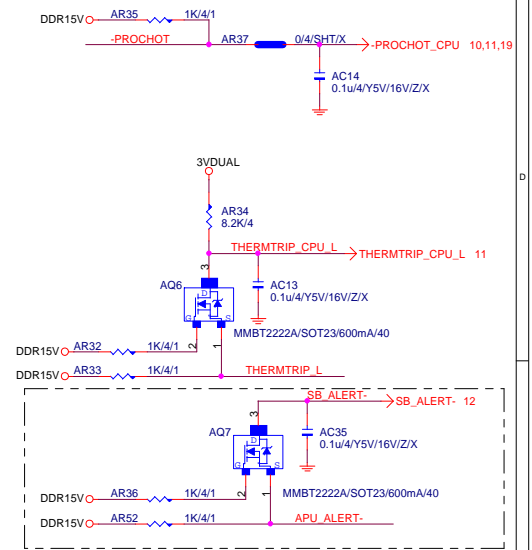
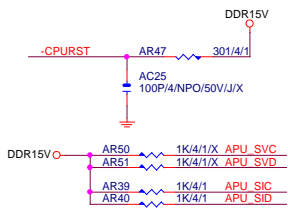
```

+1.1V_RUN=FCH_VDD_11_RUN=VCC_SB

```
+3.3V_RUN=VCC3
+3.3V_ALW=3VDUAL
```

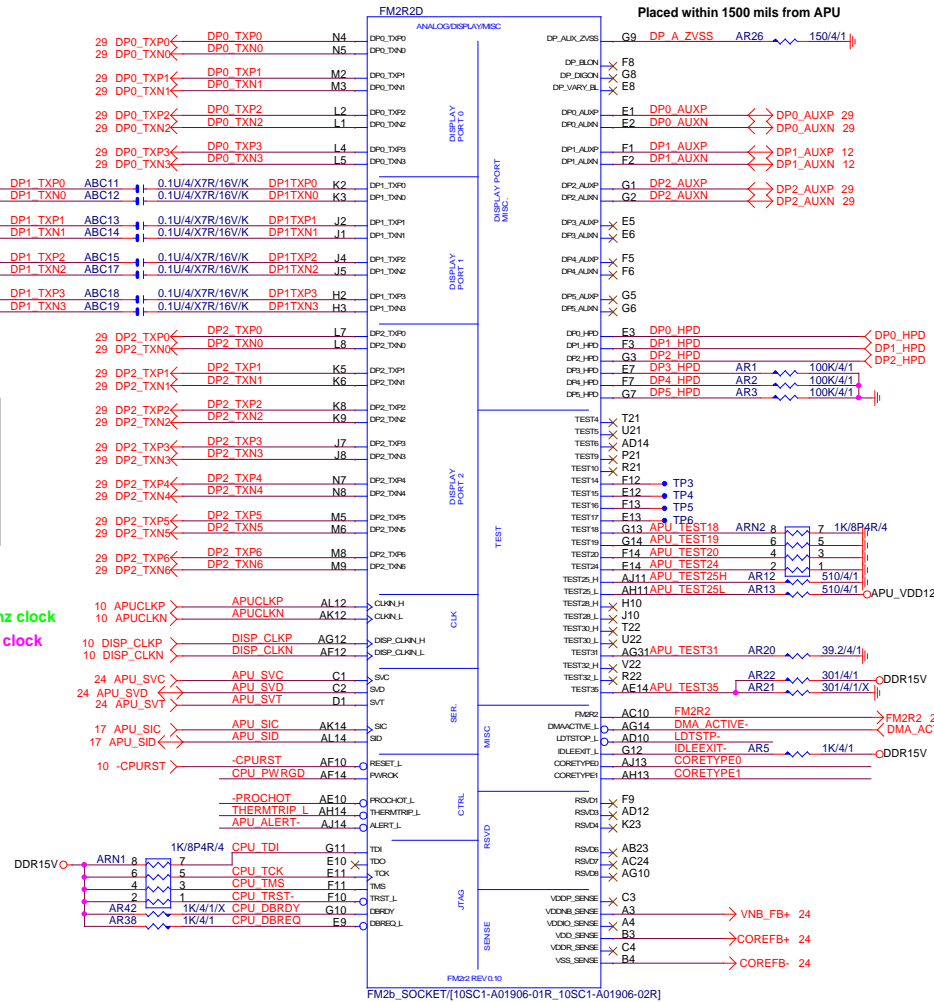
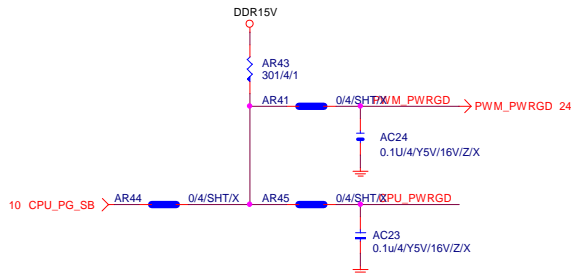




FM2 CPU Clock Layout Guide

	Impedance	4L-1080
APU Clock	85 ohm	20/4.5/7.5/4.5/20
DISP Clcock	85 ohm	20/4.5/7.5/4.5/20
DP TX/RX	85 ohm	20/4.5/7.5/4.5/20
	55 ohm	4 mil
	40-60 ohm	7 mil

APU Spread 100Mhz clock
DP Non-Spread 100Mhz clock

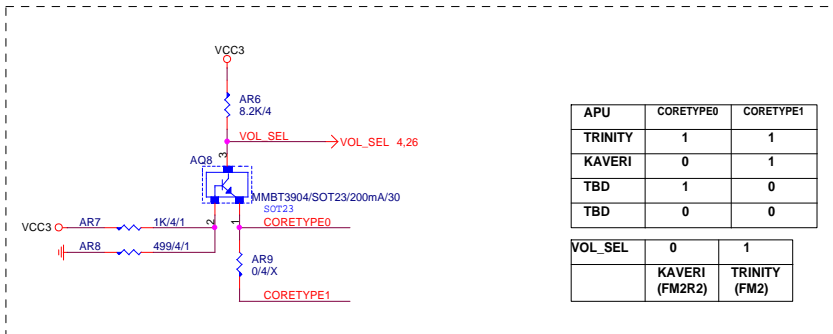


TEST35: high=>HDMI enable,
low=>HDMI disable.

FM2R2 AR31 8.2K/4/1 3VDUAL
 DMA_ACTIVE- AR30 1K/4/1 DDR15V
 LDTSTP- AR53 1K/4/1/X DDR15V
Hudson DG_1.80

	APU FM2
Group A	VDDA25:1.8~2.7V/0.5A
Group A	DDR15V:0.8~2.3V/30A
Group B	VCORE: 0.8~2.0V/120A
Group B	VCORE_NB:1.2V/50A
Group B	VDDP:1.2V/5A
Group B	VDDR:1.2V/5A

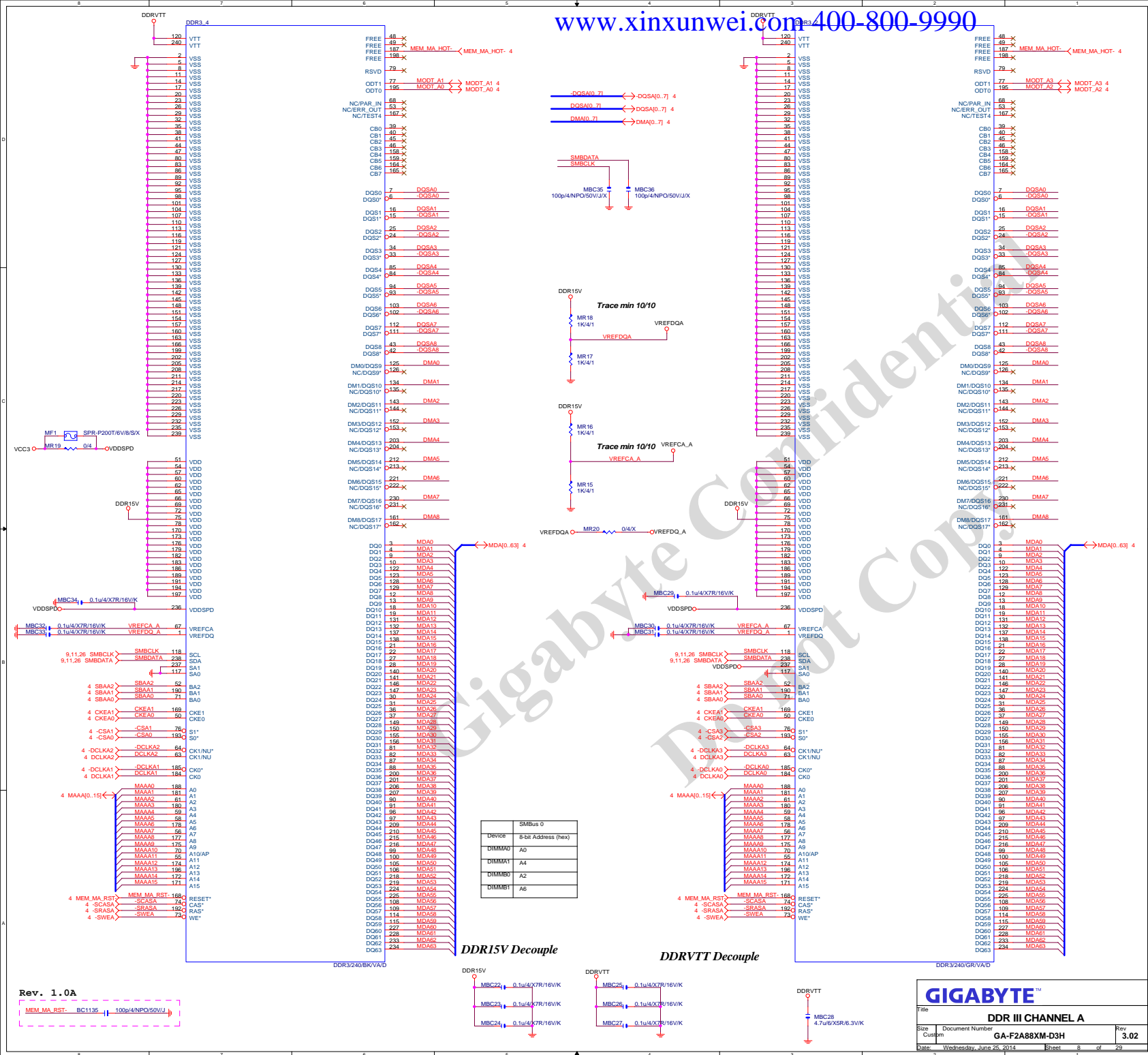
Group A must early than Group B

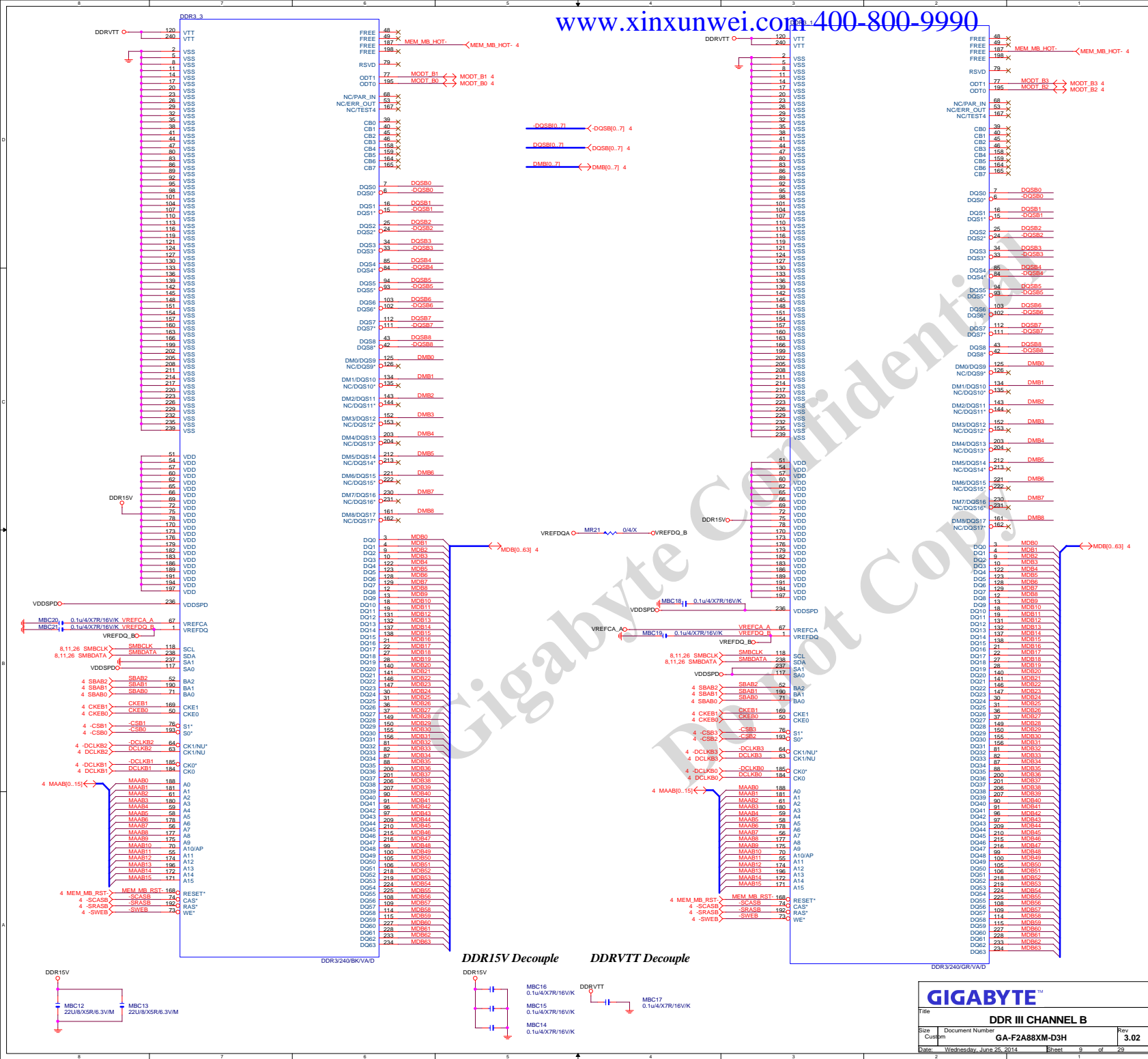


APU	CORETYPE0	CORETYPE1
TRINITY	1	1
KAVERI	0	1
TBD	1	0
TBD	0	0

VOL_SEL	0	1
	KAVERI (FM2R2)	TRINITY (FM2)

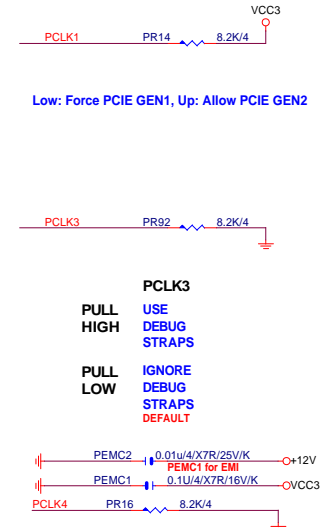
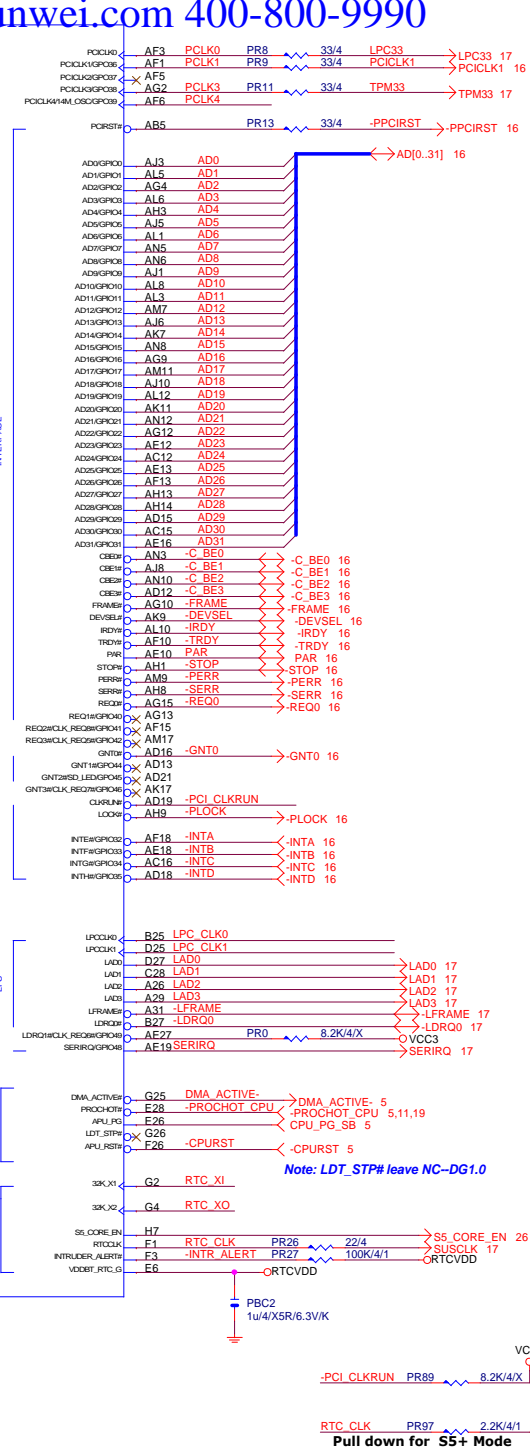
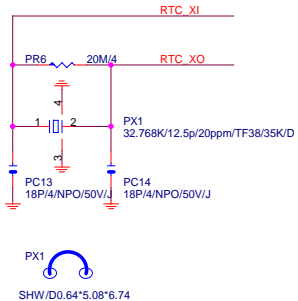
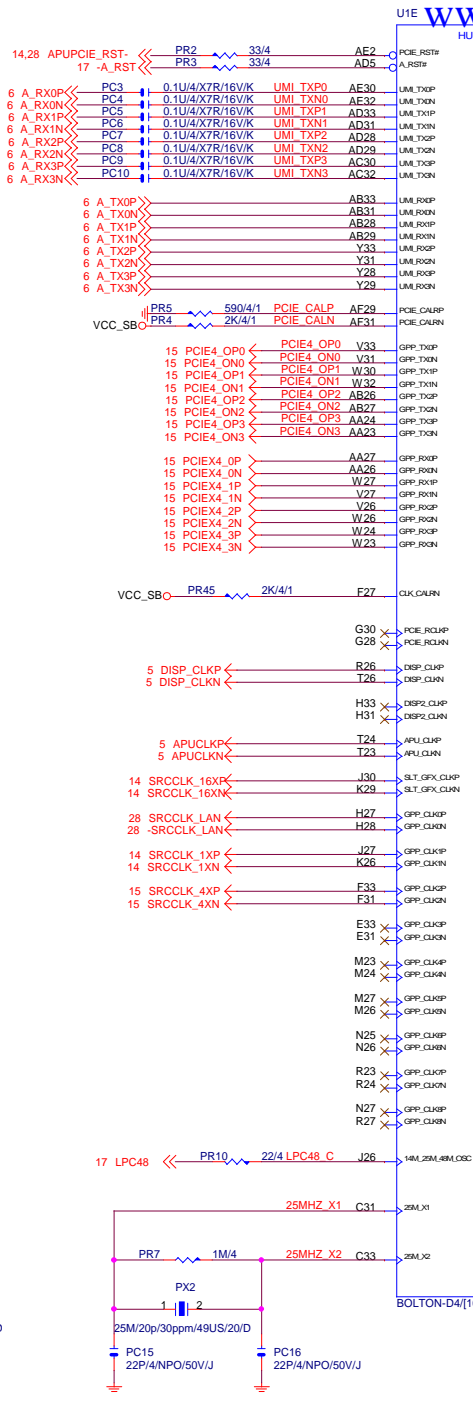
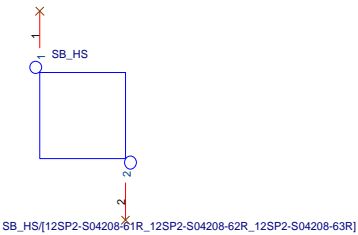




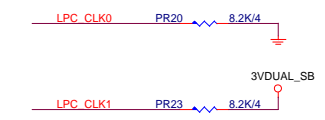


 PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

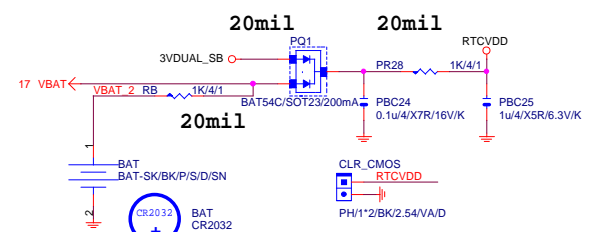
S.B HEATSINK



CLKGEN Mode: Only for integrated clock mode.



	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
	AOD Extreme	
PULL LOW	IMC DISABLED	CLKGEN DISABLED
	DEFAULT	DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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Title	HUDSON D4 PCIE/PC/CPU/LPC
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Size Custom	Document Number GA-F2A88XM-D3H	Rev 3.02
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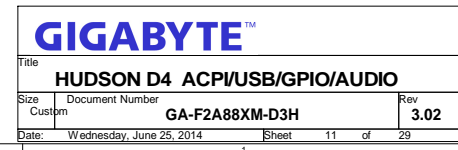
either HWM inputs or PWR_GD signals
can be used for power-up sequencer

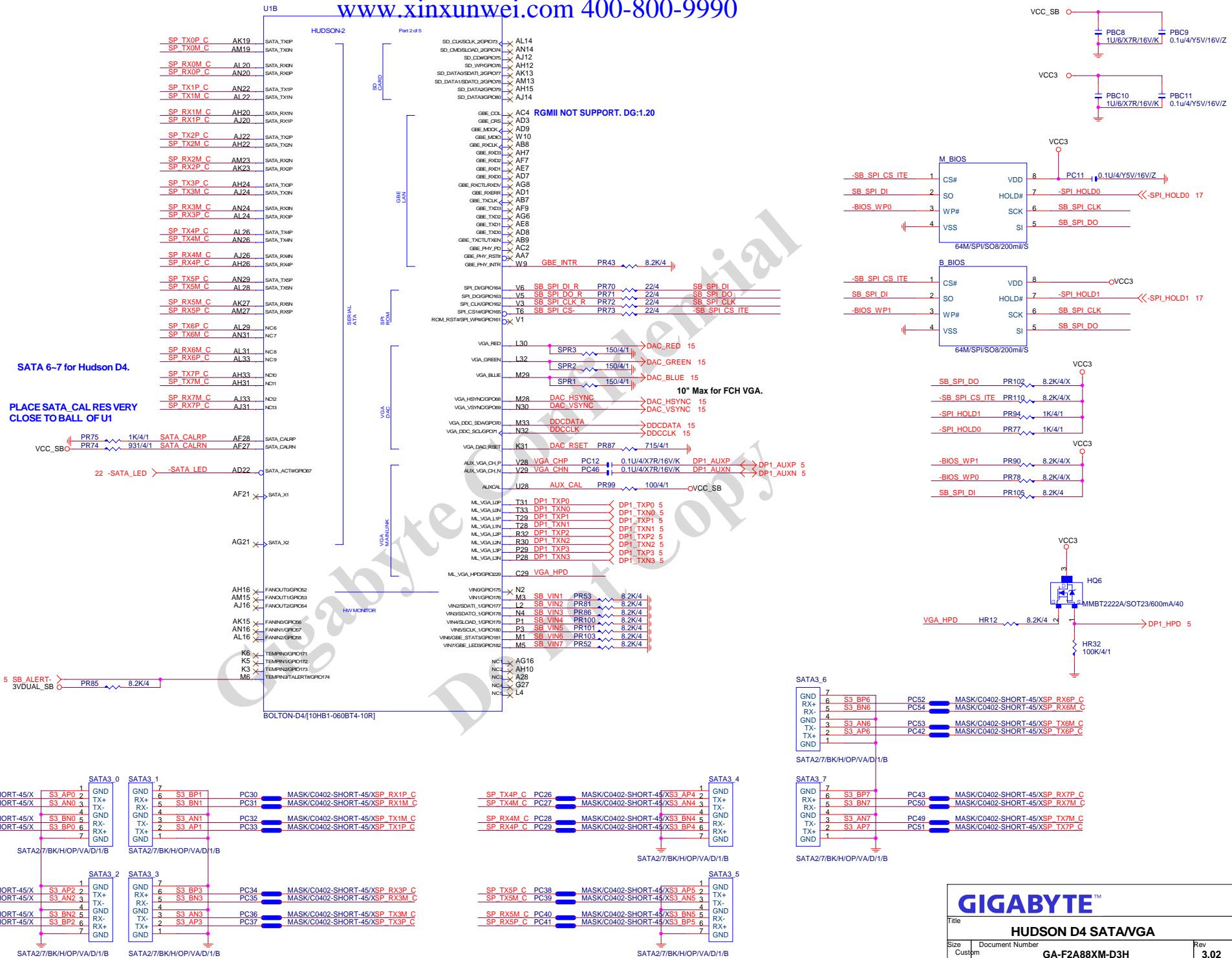
FCH_GP199 PR62 2.2K/4/1

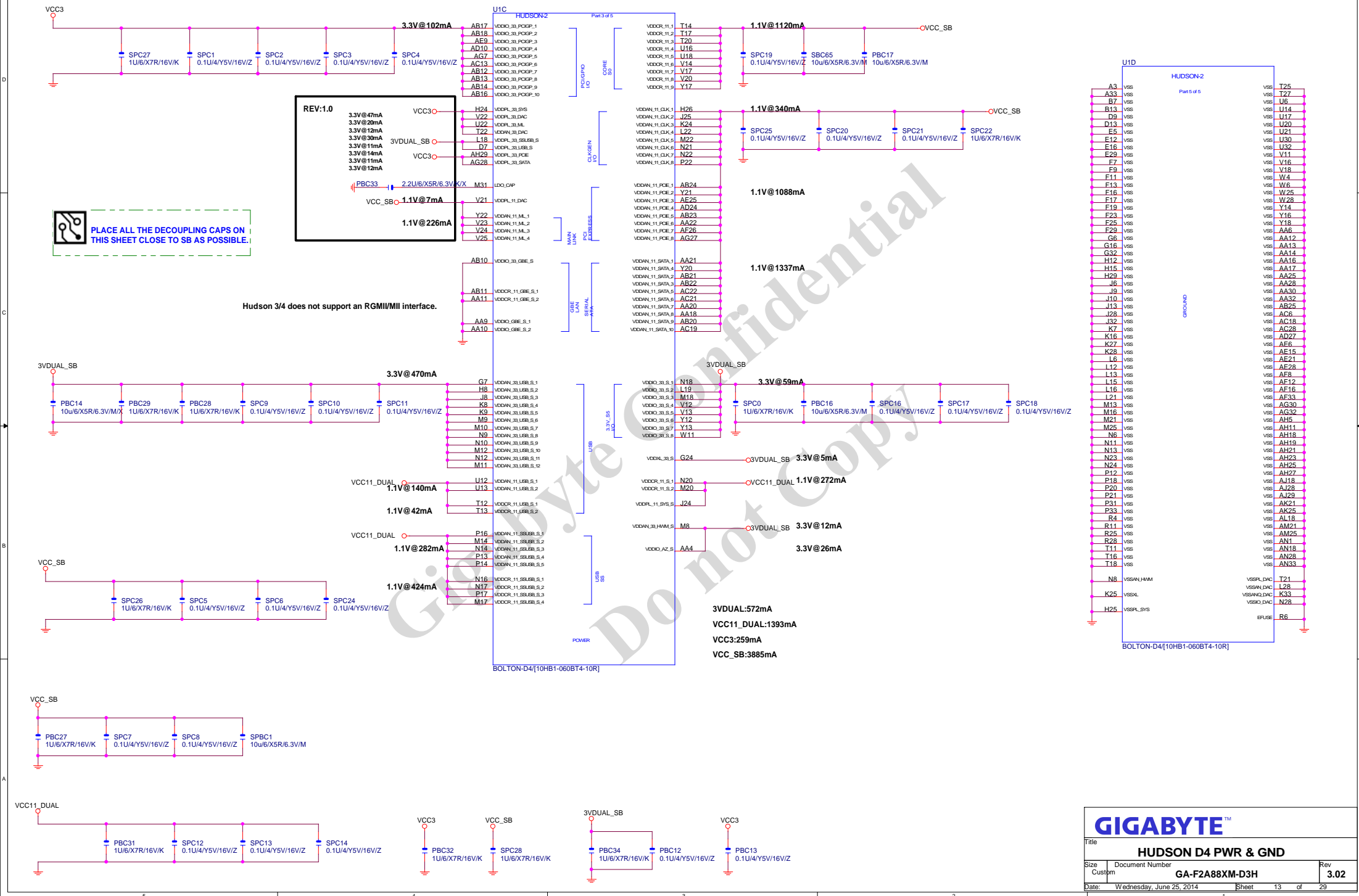
FCH_GP199

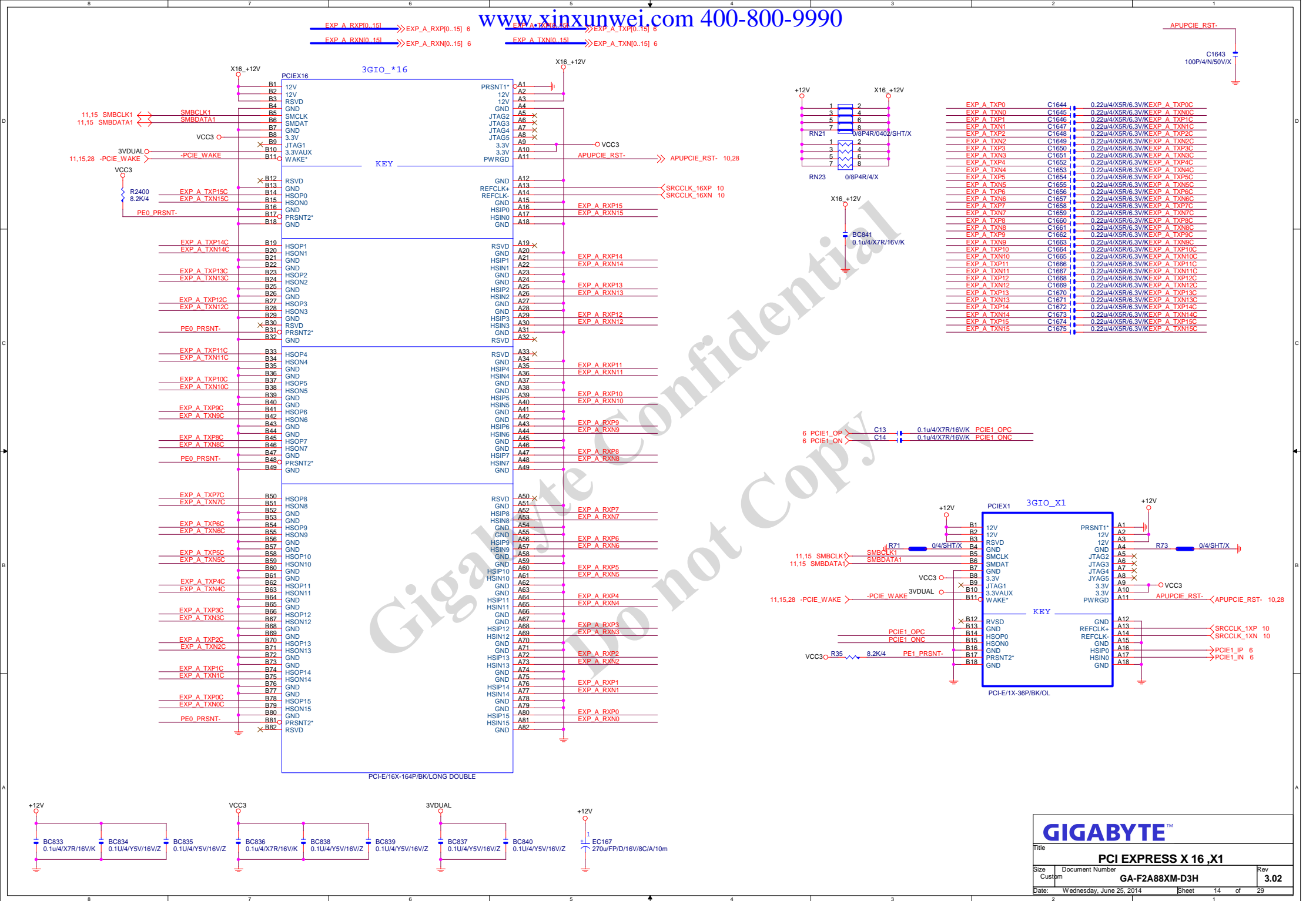
H = LPC ROM

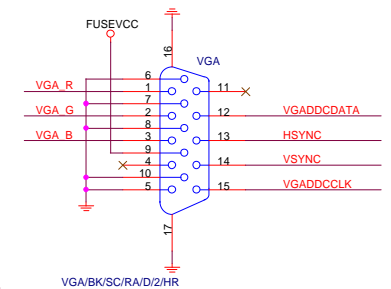
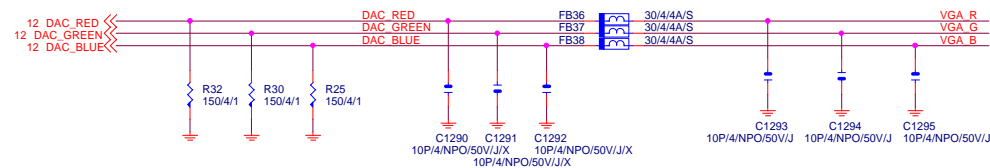
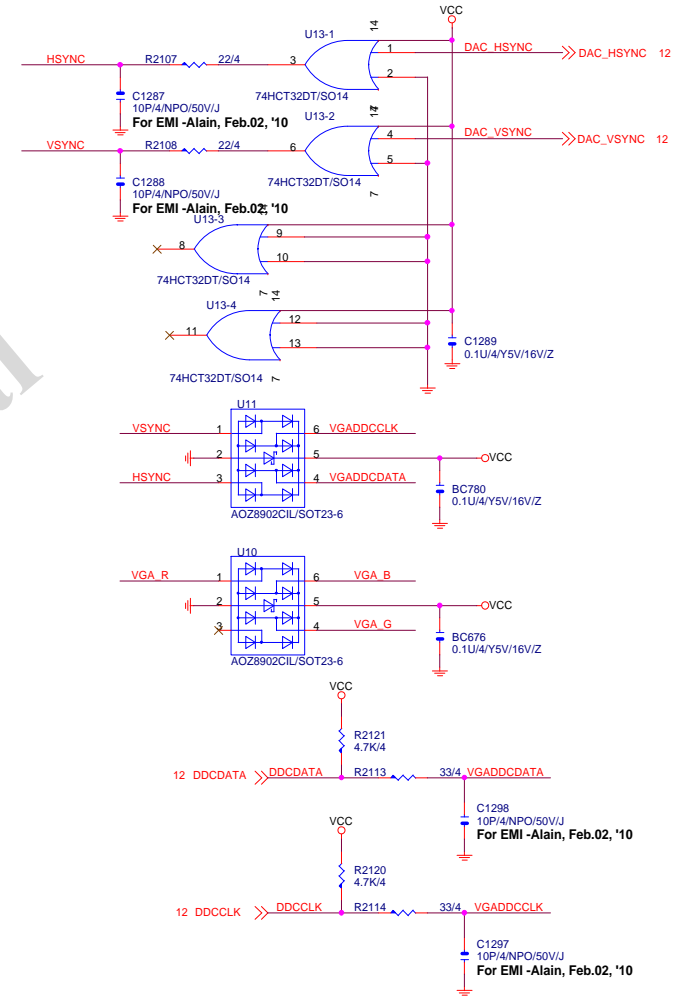
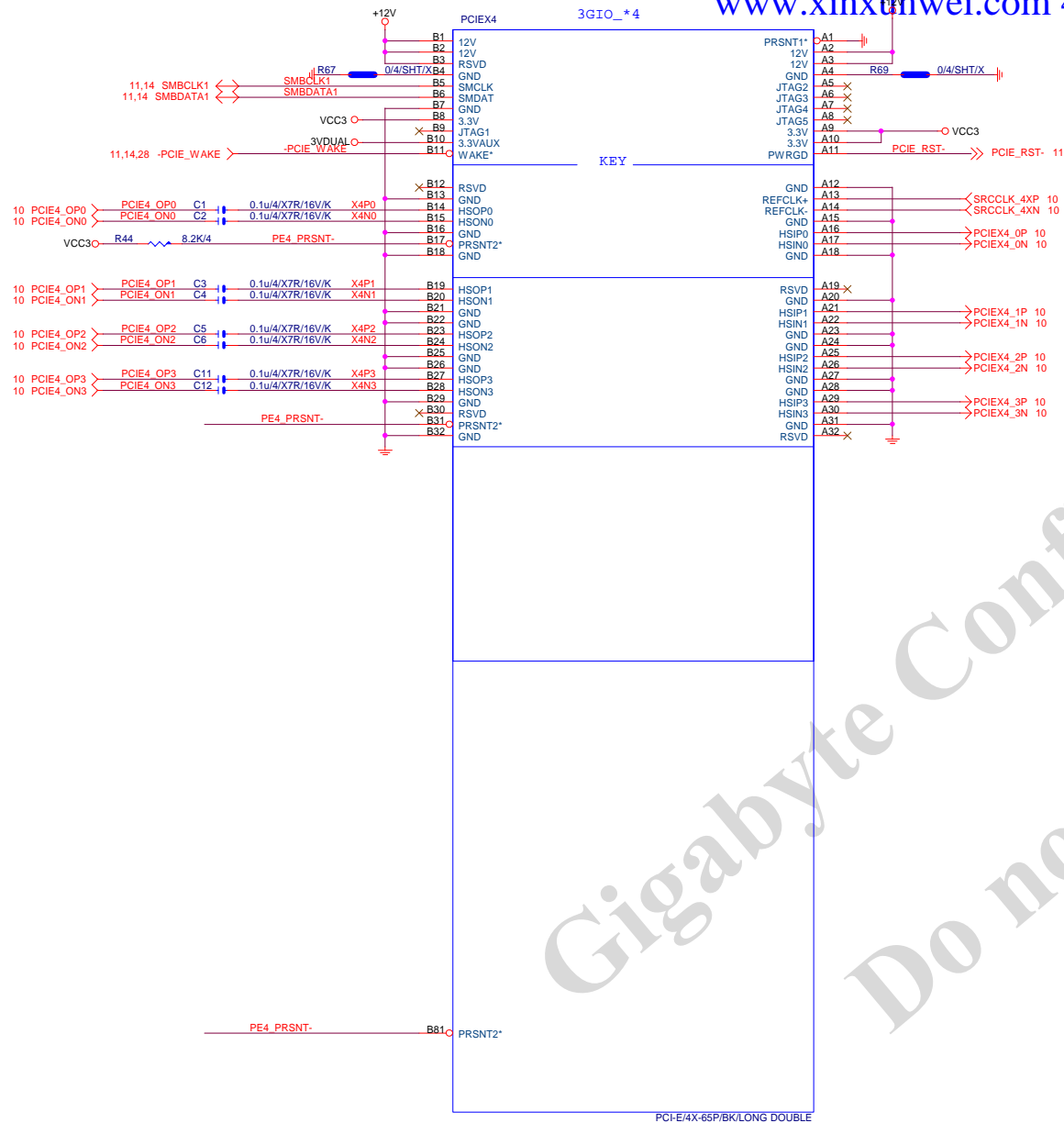
L = SPI ROM <Default>







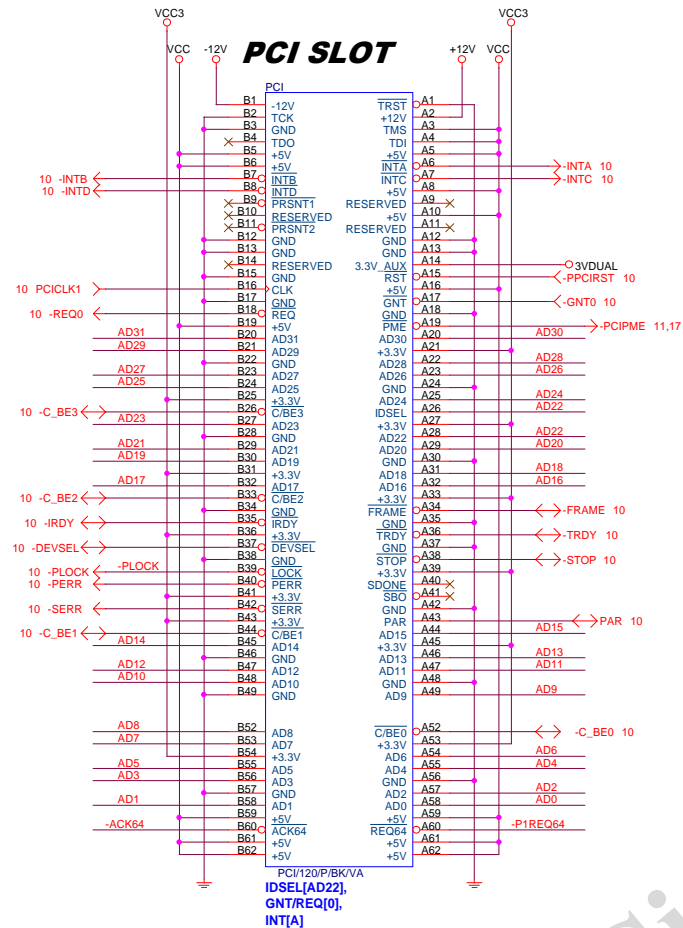




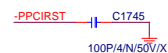
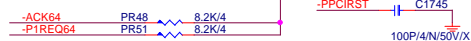
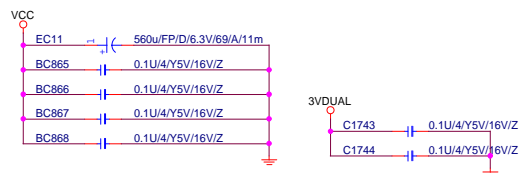
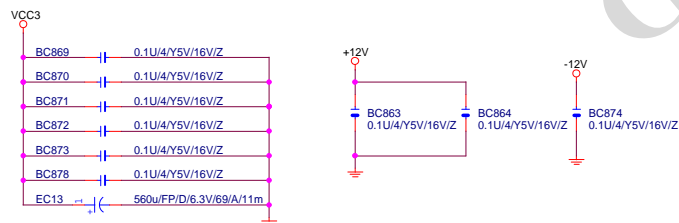
PCI SLOT 1,2

10 AD[0..31] <-> AD[0..31]

PCI SLOT



PCI/120/P/BK/VA
IDSEL[AD22],
GNT/REQ[0],
INT[A]



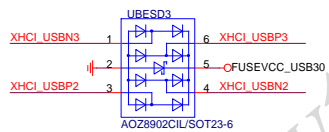
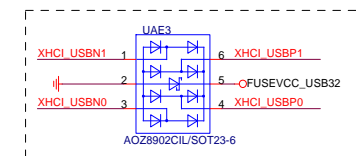
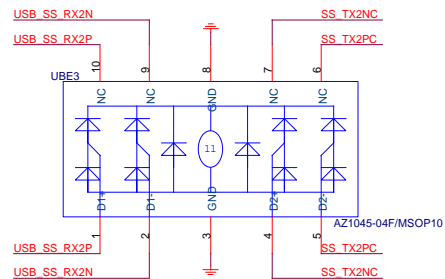
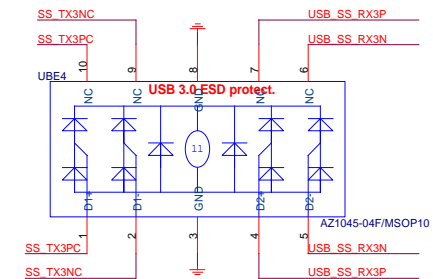
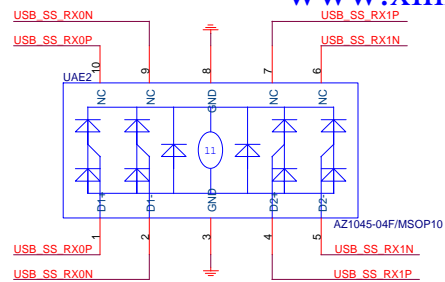
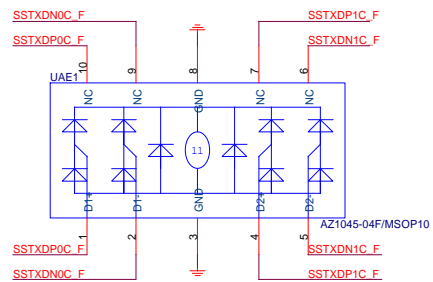
GIGABYTE™

Title

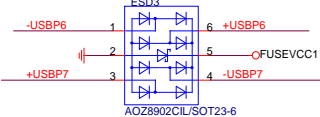
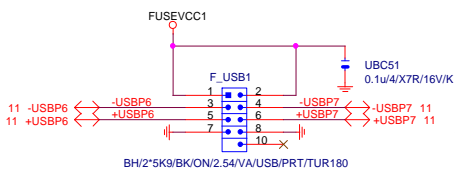
PCI SLOT

Size
CustomDocument Number
GA-F2A88XM-D3HRev
3.02

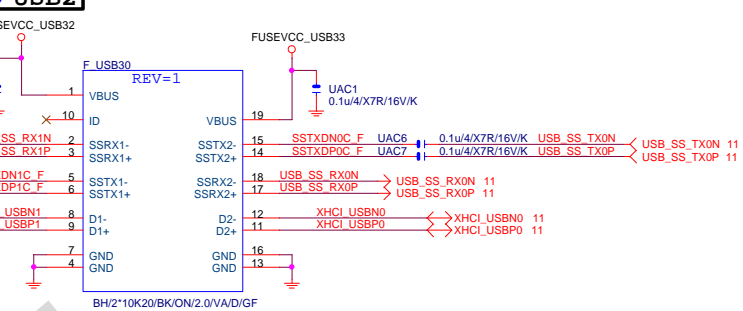
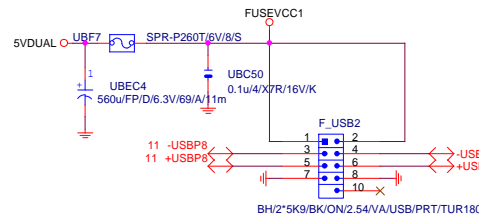
Date: Wednesday, June 25, 2014 Sheet 16 of 29



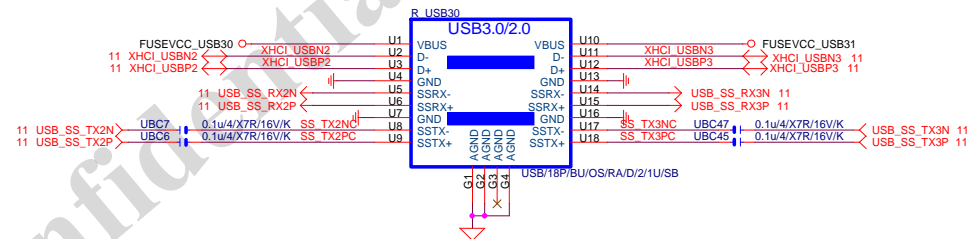
FRONT SIDE USB1



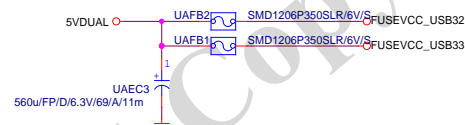
FRONT SIDE USB2



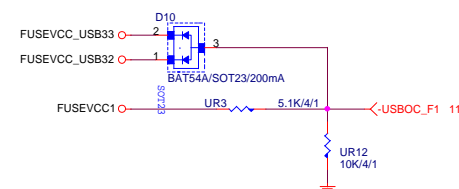
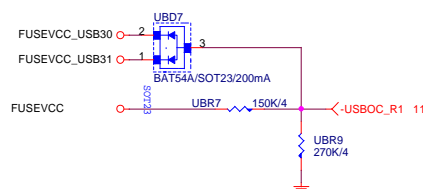
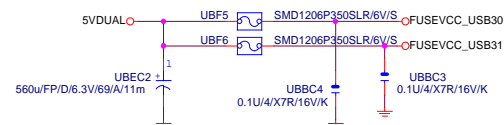
REAR SIDE USB3



FRONT SIDE



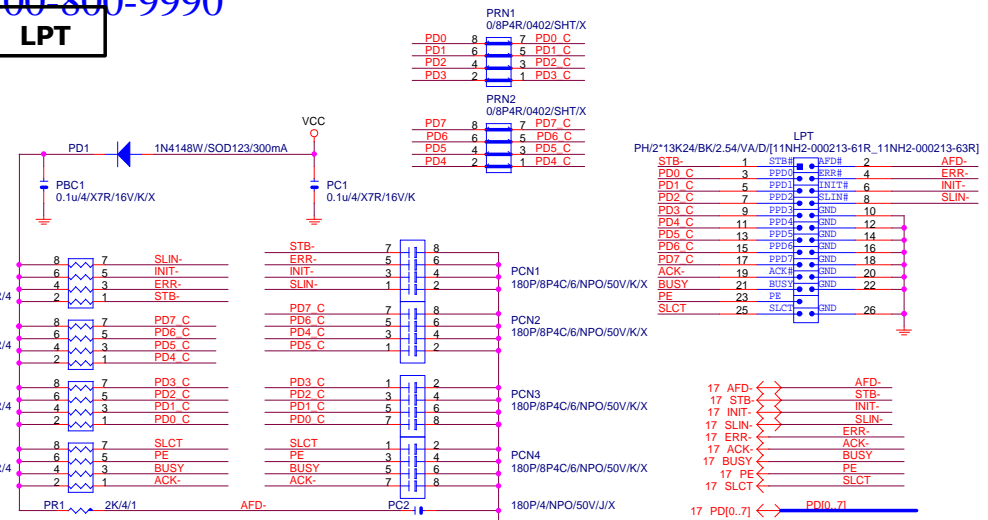
REAR SIDE



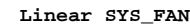
GIGABYTE™

F_USB, F_USB30, R_USB30

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Custm	GA-F2A88XM-D3H	3.02
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CPU SMART FAN

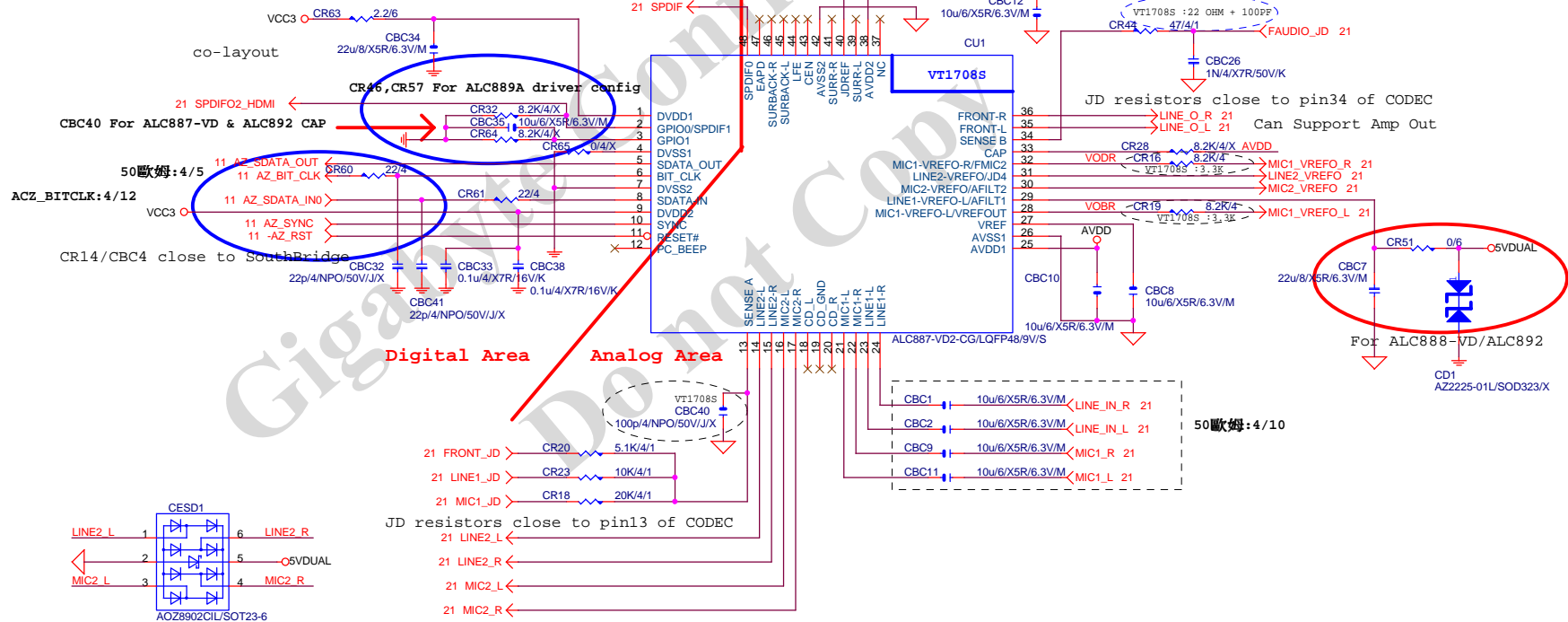


Full Turn On Function (NCT3941S-A)



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	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	O	O	X
CR64	X	X	X	O
CR44/CBC6	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR34	20K/1%	20K/1%	5.1K/1%	5.1K/1%
CR31	O	O	O	O
CR30	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CR34	20K/4/1	20K/4/1	5.1K/4/1	5.1K/4/1
CBC39/CBC40	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR1/CR14/ CR17/CR22/CR13/CR11/ CR57/CR53	75 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	O	X	X	O
CD2/CD3/CQ3/CQ5	X	O	O	X



GIGABYTE™

Title

ALC887-VD2 CODEC

Size

Document Number

GA-F2A88XM-D3H

Rev

3.02

Date:

Wednesday, June 25, 2014

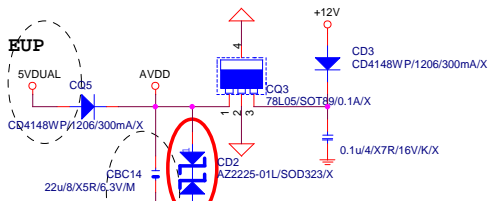
Sheet

20

of

29

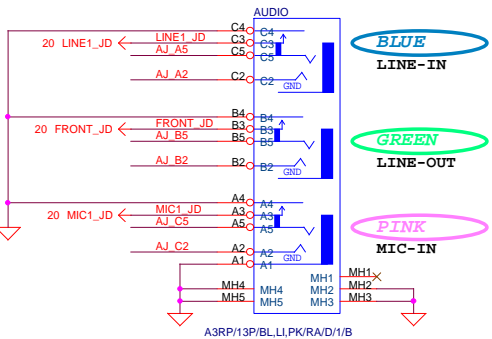
CODEC POWER/EMI PAD



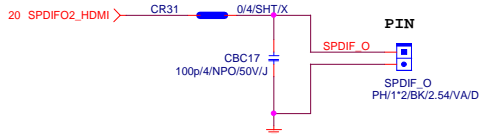
上ALC892時,此顆電容要保留

ADD CD2 For ESD PROTECT DIODE

HD Audio Jack

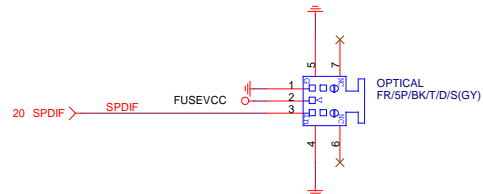


SPDIF_OUT



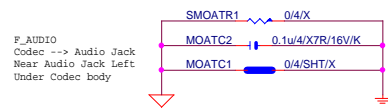
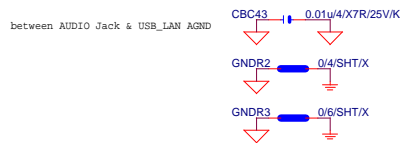
For HDMI SPDIF

2 type Connector Co-lay

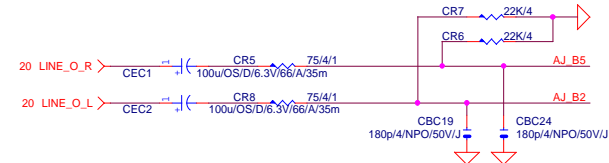


1.0/1.1 Selection

	HDMI_SPDIF	OPTICAL	CR40
Rev: 1.0	V	X	V
Rev: 1.1	HDMI	V	X

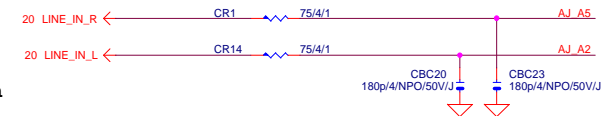


LINE-OUT



LINE-IN

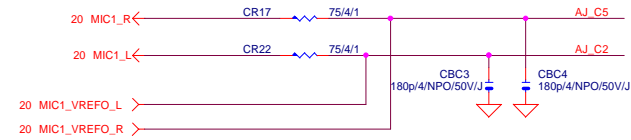
Only reserved for ALC888



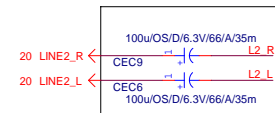
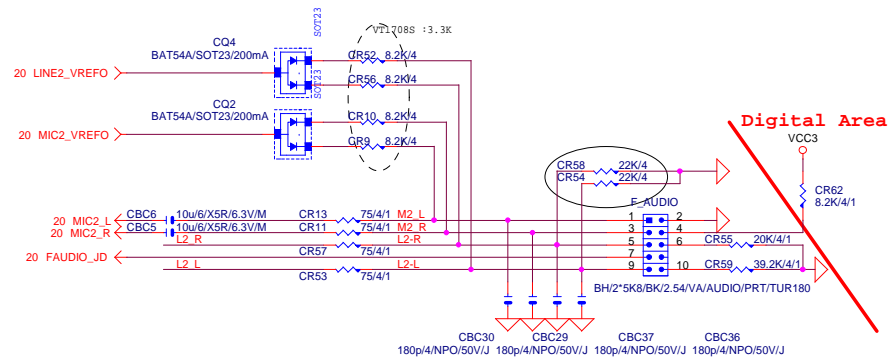
For 889A/888

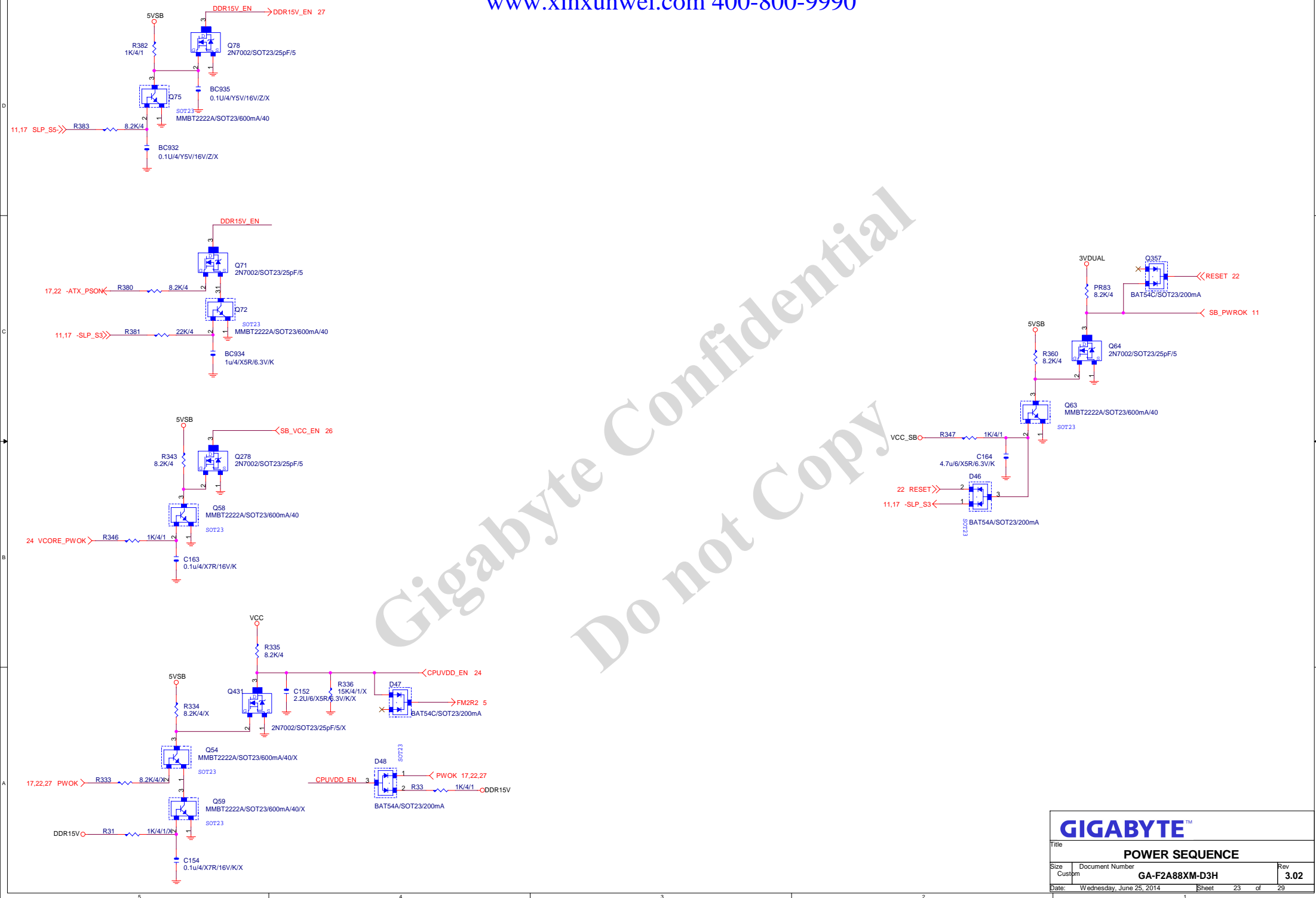
Verify MIC function
in LINE-in

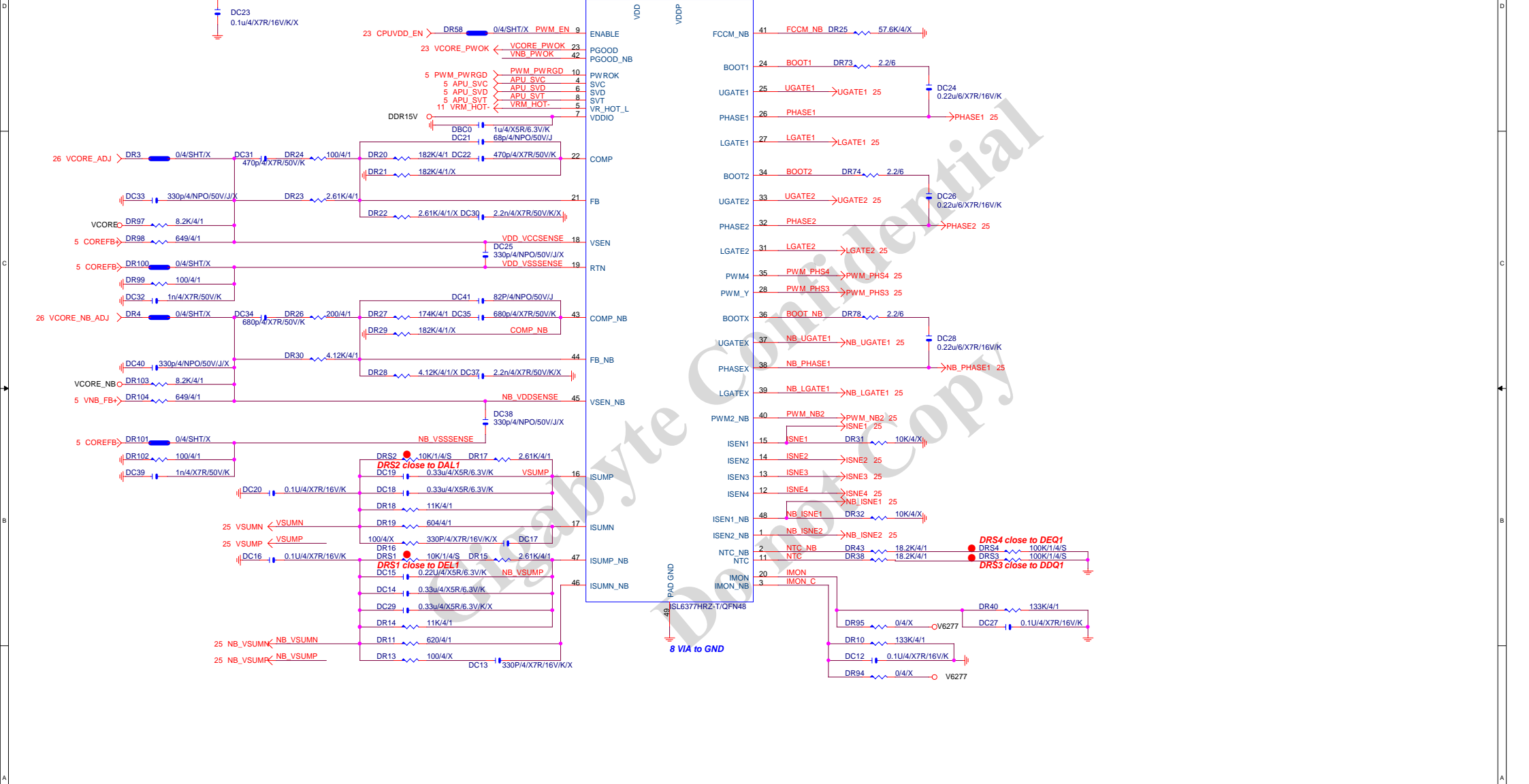
MIC-IN

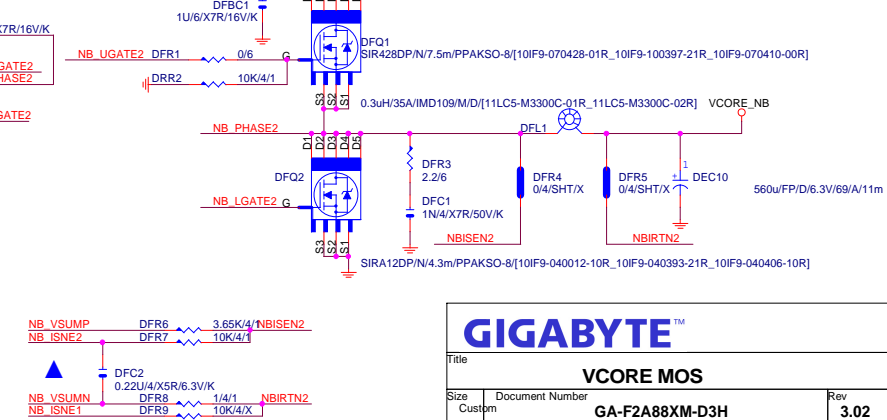
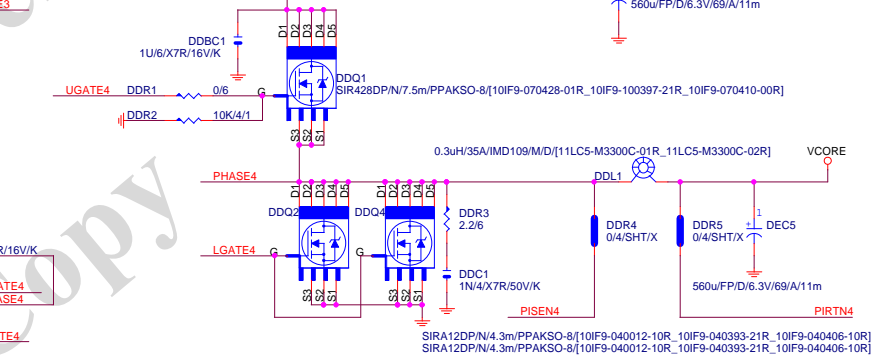
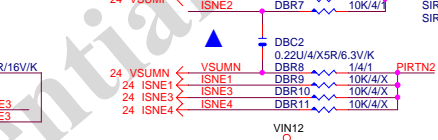
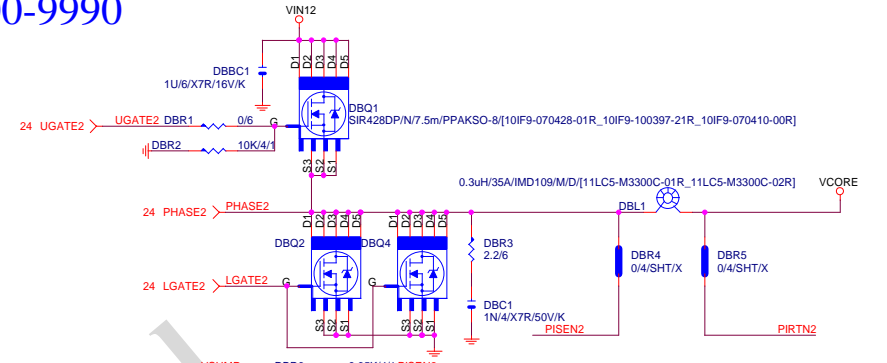
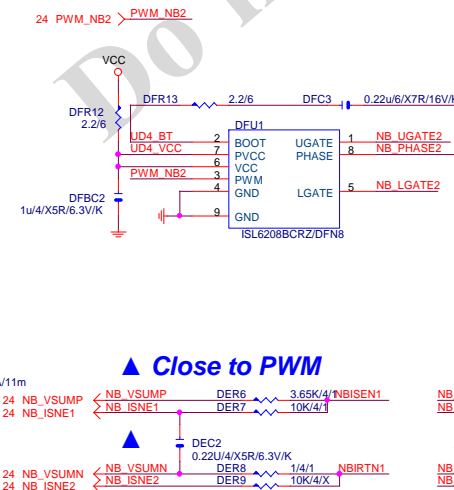
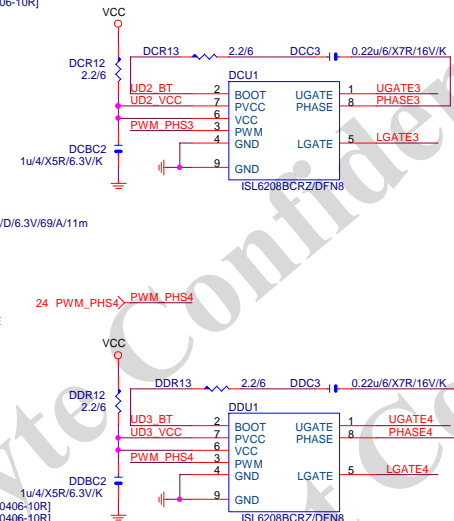
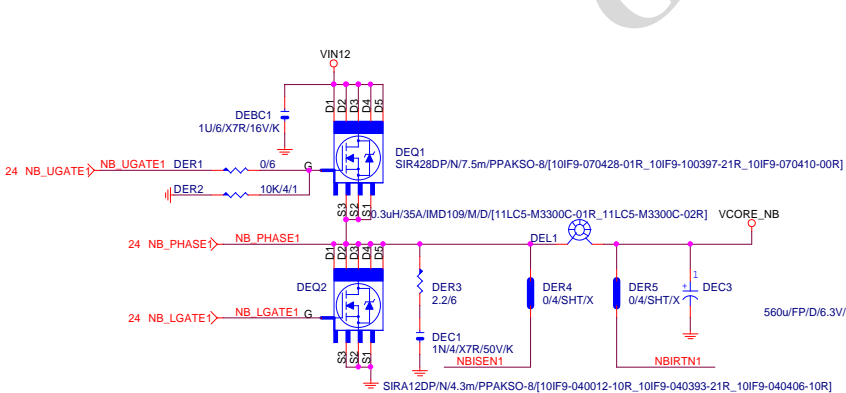
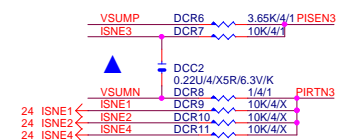
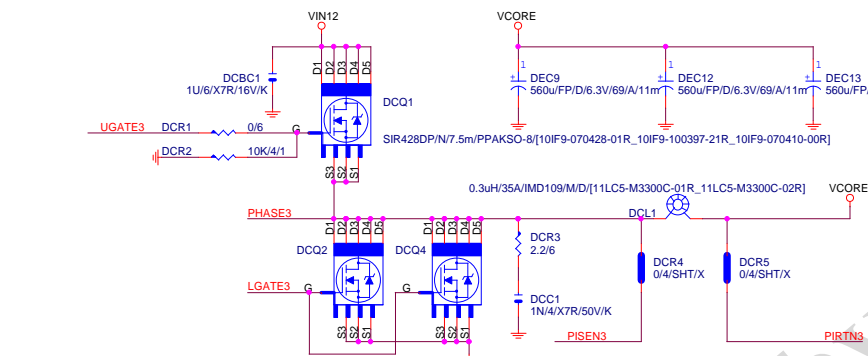
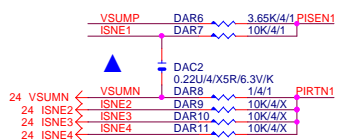
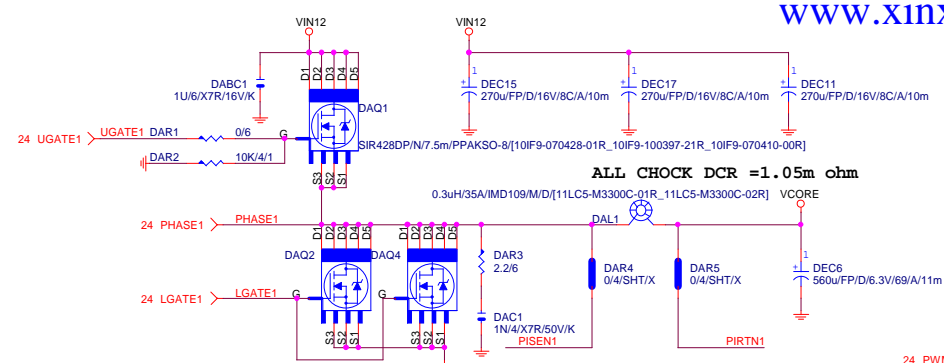


AZALIA FRONT PANEL





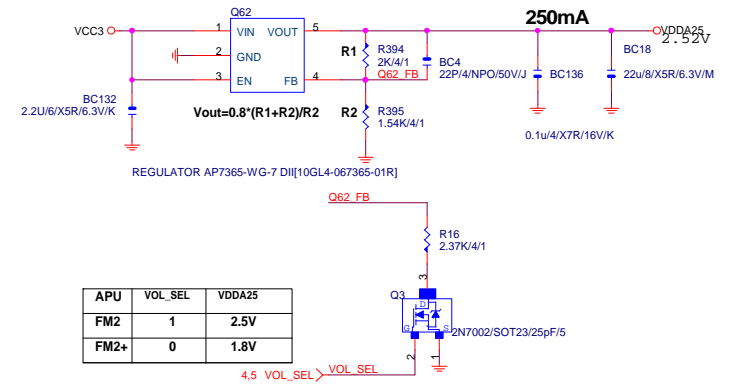
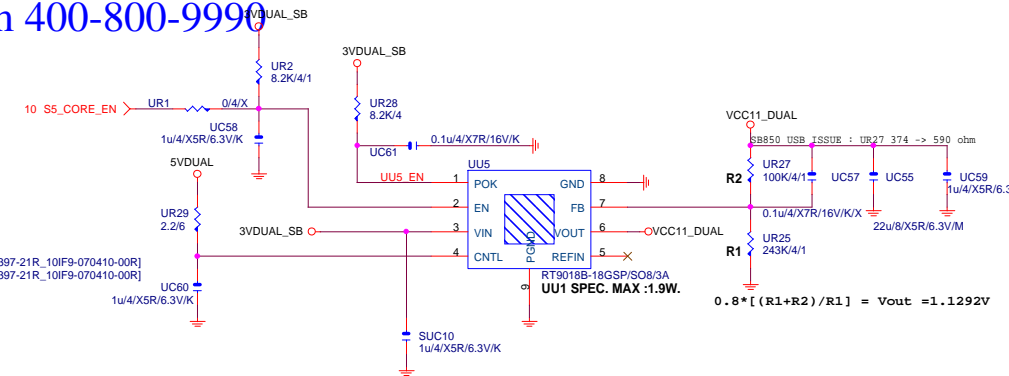
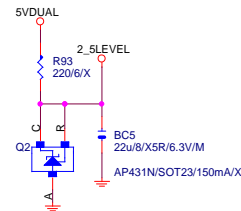
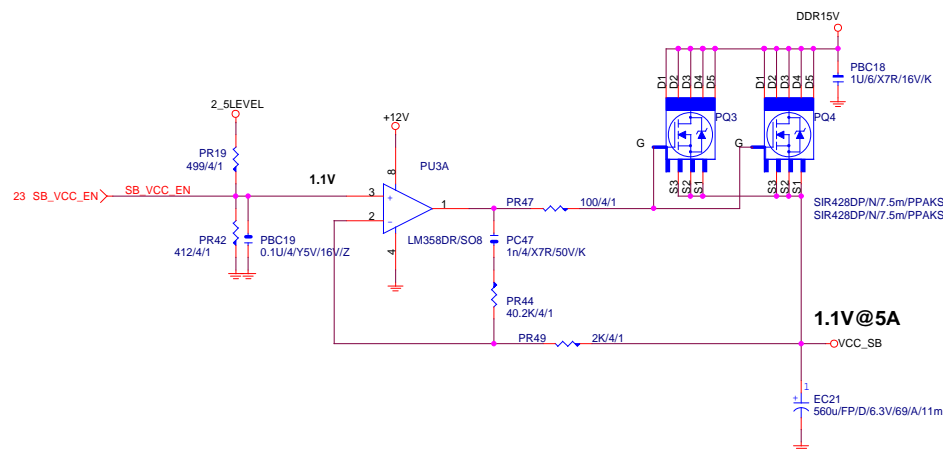




Close to PWM

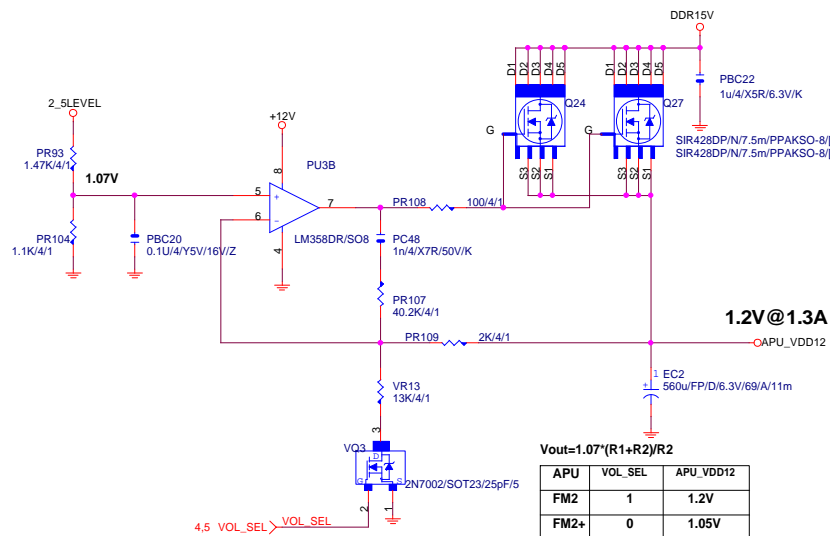
GIGABYTE™			
VCORE MOS			
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VCC_SB



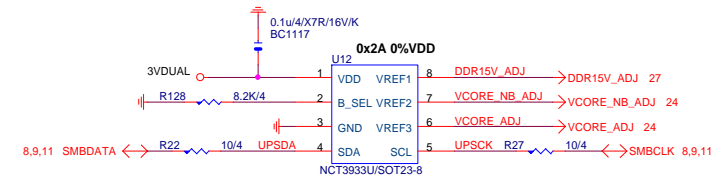
APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

APU_VDDP



$$V_{out} = 1.07 \cdot (R1 + R2) / R2$$

APU	VOL_SEL	APU_VDD12
FM2	1	1.2V
FM2+	0	1.05V

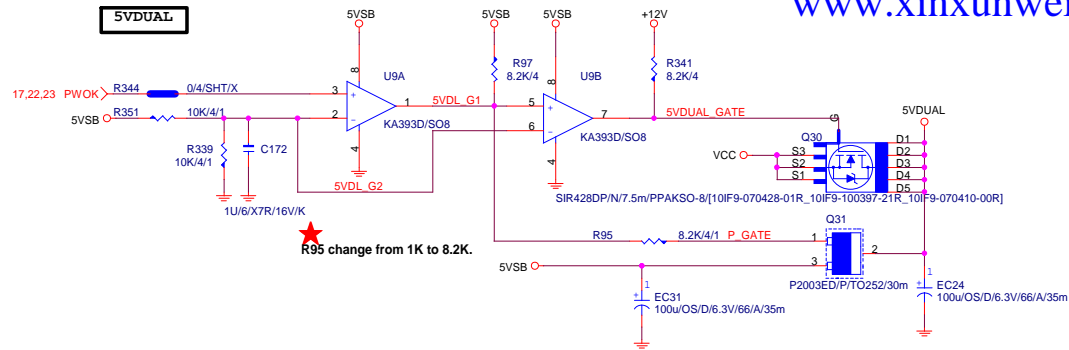


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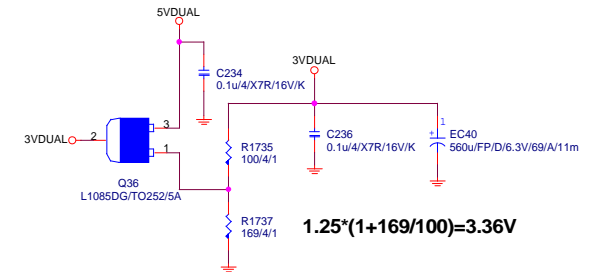
SB PWR,VDDA25,VCC11DUAL

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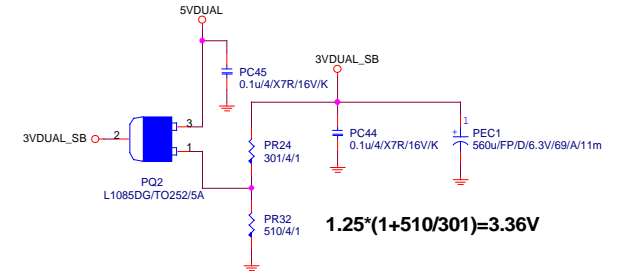
5VDUAL



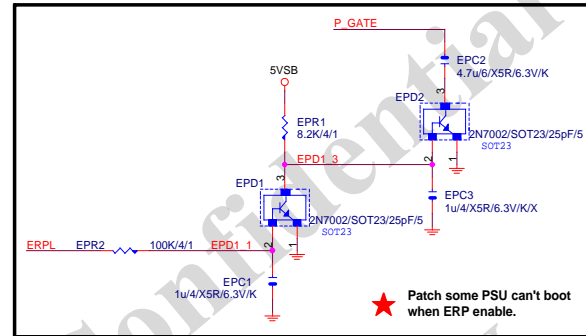
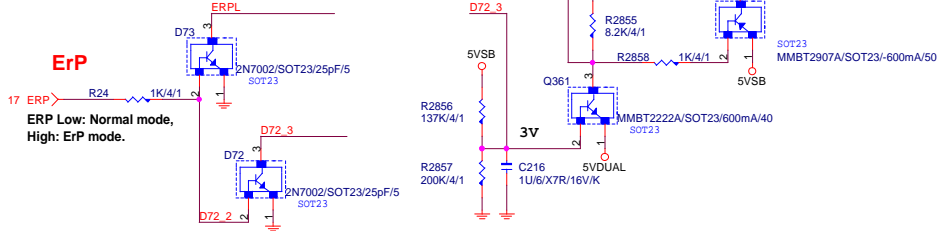
3VDUAL



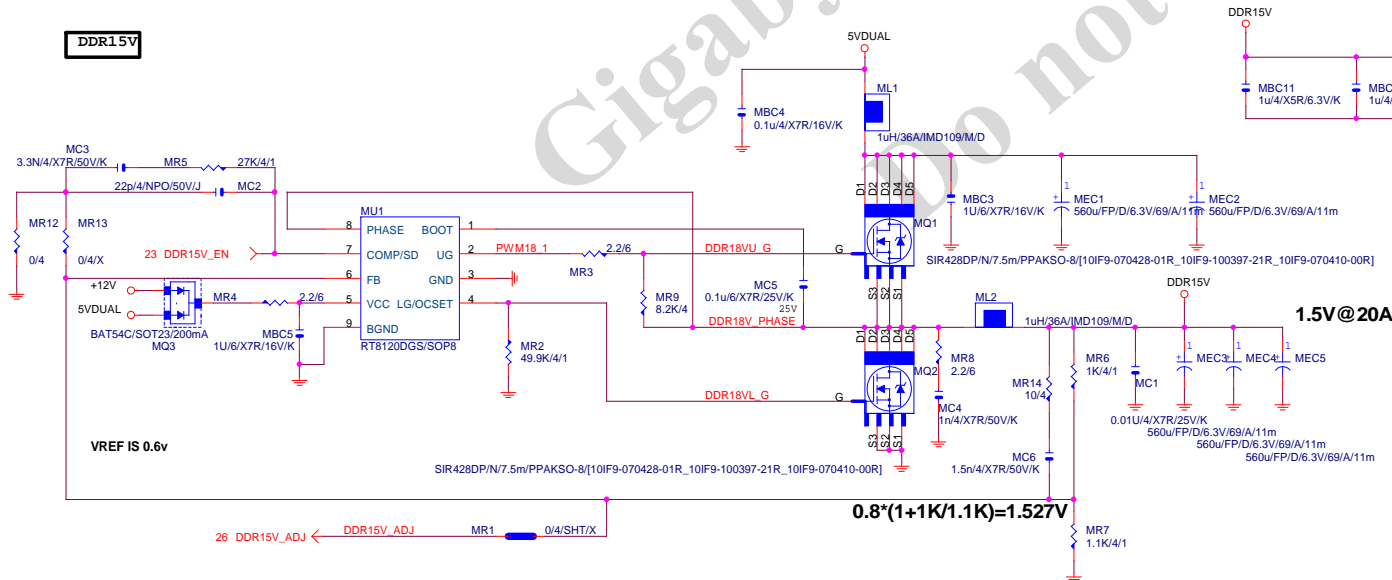
3VDUAL_SB



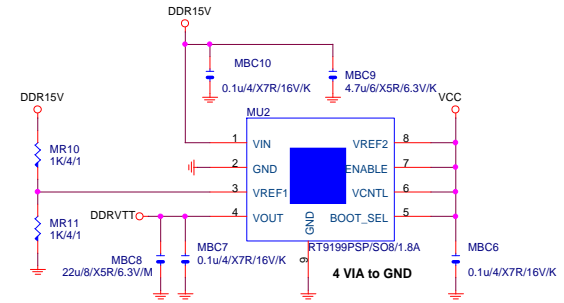
ErP



DDR15V



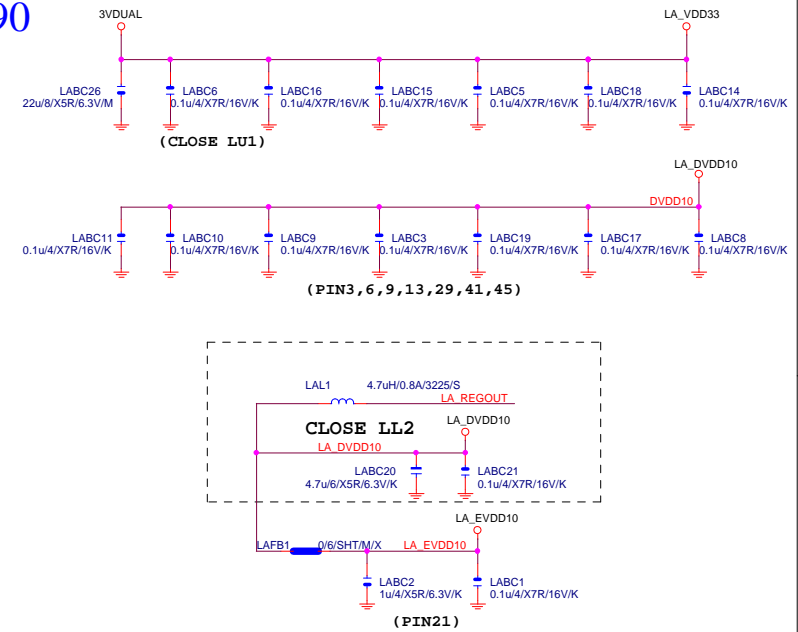
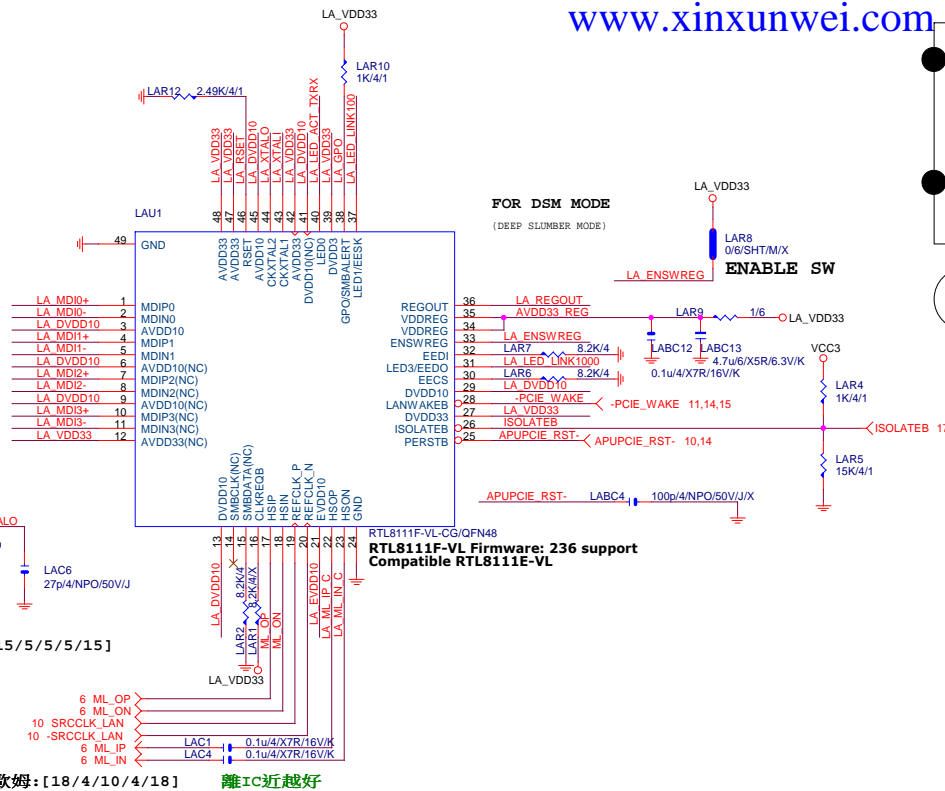
DDRVTT



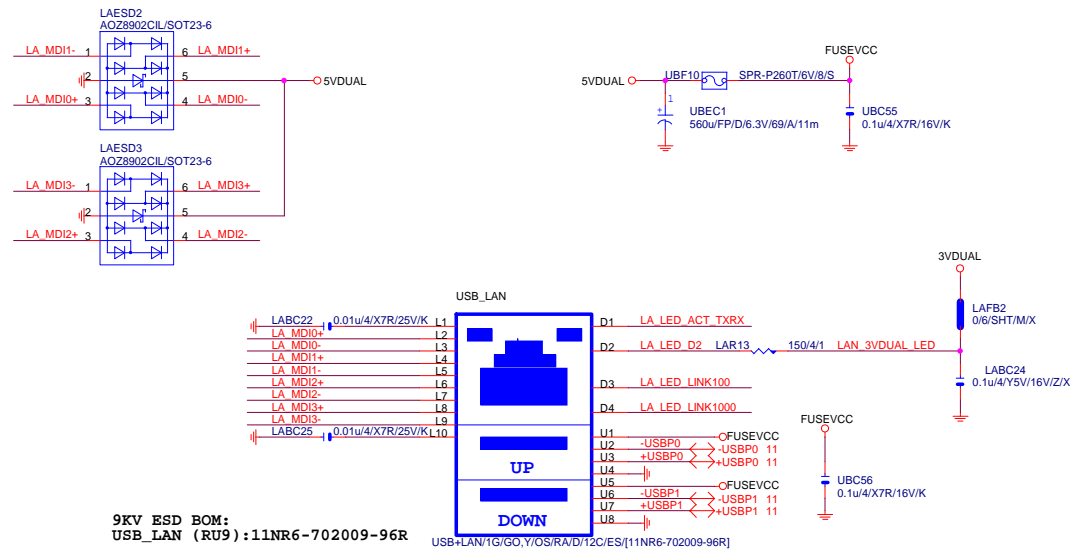
GIGABYTE

Title		
DDR PWR, 5VDUAL, ERP		
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	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



USB_LAN



使用RU9 USB_LAN可省略LAESD1保護LED

